

Product Brief

Introduction

The NetCOPE is a configurable platform which enables rapid development of network applications on the FPGA acceleration boards. The platform creates a hardware-independent abstract layer upon specific hardware boards, solves repeating tasks of network devices development such as network and host interface communication, and provides generic interface to the customer application core.

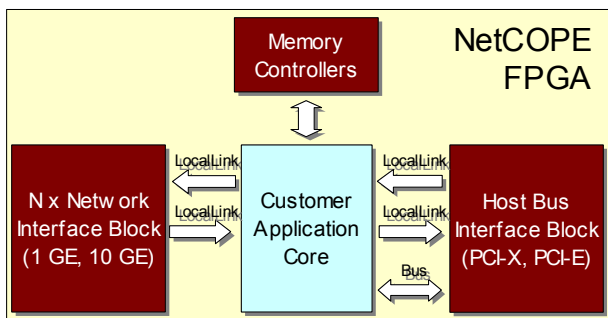
These features enable customers to design their applications in dramatically reduced time and cost as well as to achieve maximal application performance. Furthermore, it makes customer's solution independent on the specific hardware board, network physical interface and host bus system.

**“Design your application core,
NetCOPE takes care of the rest.”**

Platform Overview

The NetCOPE platform integrates hardware-dependent building blocks (network, PCI blocks) and provides configurable interface to the customer's application core. The elements of the NetCOPE platform are network interface blocks for 1 G and 10 G Ethernet, a flexible on-chip bus architecture with high speed bus master connection to the host software via PCI Express bus and a software driver. Optionally, the NetCOPE platform includes a set of IP cores for easy data manipulation, a set of memory controllers and a set of IP cores for network traffic processing. While NetCOPE resolves time-consuming performance, functional, and timing pattern issues, designers can focus on the application core – dramatically reducing costs and time-to-market for FPGA designs.

All building blocks offer uniform and clearly defined interfaces between both the NetCOPE platform and a customer application core in the FPGA, and the NetCOPE driver and user PC application. These interfaces enable customer to effectively implement applications in both hardware and software.



Features

- High performance scalable platform for rapid development of FPGA applications
- Complete network and host interface solution
- 1 G and 10 G Ethernet support
- PCI Express x1, x4, x8 support
- Reduced time-to-market and costs for user's application
- Support for COMBO boards, other cards on demand
- Comprehensive FPGA design framework
- Generic communication interfaces
- Flexible on-chip bus architecture with DMA support
- Up to 8 DMA channels option
- Device drivers included

FPGA Application Core Interface

The communication with the network interfaces is performed by the Network interface blocks, which support 1 G and 10 G Ethernet. Incoming packets are forwarded to the application core using Xilinx LocalLink protocol format. The communication with host bus interface is performed by the high performance On-chip interconnection system (ICS). This flexible bus architecture includes a host bus interface bridge, a high-throughput Internal bus, a resource-saving Local bus and DMA controllers. The ICS allows to connect arbitrary number of user components and provides a simple LocalLink interface for fast packet transfers between the FPGA application core and the host software driver.

Software Interface

The NetCOPE software includes a set of development tools, a communication library and device drivers with well-defined interfaces. The customer can use both single read and write operations and DMA transfers to access the FPGA application core. The device drivers allow fast packet transfers between the application core and software application via standard system network interface or via application specific interface.

Target Applications

- Networking and Telecommunications (monitoring, IDS/IPS, VoIP applications, cryptography)
- High-performance I/O applications (multimedia, security, bioinformatics, etc.)

Hardware Independent Abstract Layer

Usage of existing hardware platforms is one of the most common approaches to shorten product development. Unfortunately, each vendor provides different customer's solution support. Most of the vendors don't provide a complete design environment including network interface blocks, host bus solution, memory controllers, drivers etc. As a result, customers are obliged to design these parts themselves or to buy and customize an appropriate third party IP cores. Such process is very time-consuming and brings the risk of losing all the effort when a board vendor comes up with new platform with its new specifics.

The NetCOPE platform solves these drawbacks and provides complete design environment to support customer's application. It creates hardware-independent abstraction layer with identical interface for all supported hardware boards. Our customers benefit from this approach as a support of new hardware platforms is added with a limited effort enabling short time-to-market and easy support for many FPGA boards.

Complete PCI Express Solution

The On-chip interconnection system provides integrated PCI Express solution. The host bus bridge allows easy interconnection with the Xilinx Endpoint block plus for PCI Express or other vendors host bus endpoints. The Internal bus and the Local bus perform data transfers between FPGA components and the host RAM, and between FPGA components internally. The Internal bus supports full PCI Express x8 throughput whereas the Local bus is resource-saving and allows to connect large number of components, which don't need high throughput to the software layer.

Optional IP Cores

The NetCOPE platform optionally includes a set of IP cores for easy data manipulation (LocalLink tools), a set of memory controllers and a set of IP cores for network traffic processing.

The LocalLink tools are an extensive set of components which help designers with data stream manipulation. The components of the LocalLink tool set perform operations like data stream splitting or switching, data streams merging, data width transformations, frame marking, frame field extracting, etc. All components of this set are fully configurable.

The IP cores for network traffic processing include high precision time-stamping unit, processors for packet analysis, classification and editing, packet queues, pattern matching units and others. The controllers for DDR SDRAM, DDR2 SDRAM, SRAM, QDR SRAM, TCAM or FLASH memory could be also included. Please contact INVEA-TECH for further information about these IP cores.

Software Driver

The software driver is designed in such a way that the hardware is abstracted. This means that the customer's application is independent of whether it operates upon 4 x 1 G optical platform, a 1 x 10 G platform or any other. This simplifies and reduces the customer's work to support multiple HW boards.

The device driver allows fast packet transfers between the application core and software application via the standard system network interface or via the application specific interface. In the first approach, each physical network interface is registered in the operating system and software application accesses the FPGA board as a standard NIC. In the second approach, packets are transferred directly to the application in a raw format including additional control data (timestamps, etc.).

Supported Hardware Boards

The NetCOPE platform is available for all INVEA-TECH COMBO boards. Any other board can be supported upon your request.



COMBO 4x1GE
INVEA-TECH

COMBO 2x10GE
INVEA-TECH

Your card
?

Platform Usage

The NetCOPE can be used as a base platform for development of customer's application to reduce its cost and time-to-market. The customer can also submit the whole design to be made by INVEA-TECH as a custom-made application.

Deliverables

- Fully synthesizable NetCOPE IP cores
- VHDL simulation models
- Complete documentation
- Synthesis scripts
- FPGA board drivers and Reference designs
- Expert technical support

Ordering Information

The NetCOPE platform is provided under terms of the SignOnce IP license. Please contact INVEA-TECH for pricing and additional information about this product.

This product is based on the technology transfer from CESNET z.s.p.o.