

Product Brief

Introduction

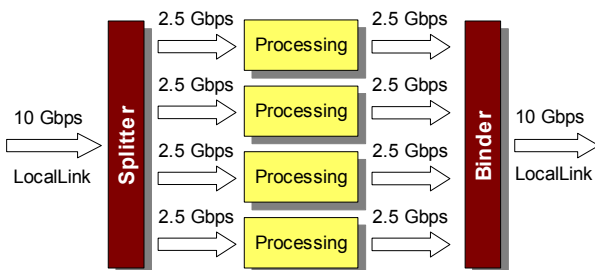
The LocalLink protocol, introduced by Xilinx, is defined as a high-performance, synchronous, point-to-point connection protocol designed to serve as a user interface to system-level Xilinx intellectual property designs. It is also suitable for connection of user components, because it is effective and widespread among IP core vendors.

The LocalLink tools are a set of components which help designers with data stream manipulation and enables customers to design their applications in reduced time and cost. The components of the LocalLink tool set perform operations like data stream splitting or switching, data streams merging, data width transformations, frame marking, frame field extracting and also provide support for data storage and IP cores debugging. All components of this set have configurable data width and configurable number of interfaces to facilitate its exploitation in various situations.

Example Application

Data distribution and parallel data processing are common tasks in many FPGA systems. These tasks are easily accomplished by Splitter and Binder components. The Splitter allows to distribute one input data stream to an arbitrary number of output data streams with lower throughput. Vice versa, the Binder allows to merge an arbitrary number of input data streams to a single high-throughput data stream.

The example of usage is line-speed packet processing on 10 gigabit Ethernet. The input data from a 10 GigE MAC core are distributed into four packet streams and processed by four parallel processing units. The required throughput of each unit is 2.5 Gbps. The processed data are merged together by the Binder component and transmitted via the output 10 gigabit interface subsequently.



Parallel stream processing using LocalLink Splitter and Binder.

Features

- Extensive tool set for various data manipulation tasks
- Supported operations: data streams splitting, merging, switching, transformations, frame field extracting, frames marking, trimming and much more
- Compliant with Xilinx LocalLink protocol
- Configurable number of input and output interfaces
- Configurable buffer sizes
- Supports configurable interface data widths of 8 to 128 bits
- High operational frequencies
- Wide variety of tools:
 - Data flow processing components
 - Data storage components
 - Others components
- Debug and simulation support for components with LocalLink interface

LocalLink Splitter

LocalLink Splitter is a component for splitting packet data flow (according to the LocalLink protocol) from one input interface to arbitrary number of output interfaces. Both, data widths and number of output interfaces are configurable. The output queue is chosen according to the least-used-queue policy. It means that incoming frame will be redirected to the output queue with the least occupied space. This algorithm ensures required output flow balancing. The Splitter is very useful when there are components with different throughput in the processing chain. It can be used to split output data flow from one fast component to several slower parallel components.

LocalLink Binder

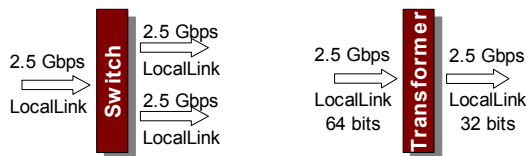
LocalLink Binder is a component for merging packet data flows from several input interfaces into one output interface. Both, the number of input interfaces and input/output data widths are configurable. There are two optional algorithms for input queue selection: Most Occupied - the input queue with most occupied space is chosen for output and Round Robin - a fair algorithm which applies round robin on input queues. The example of this component usage is merging of data streams previously created by the Splitter, or binding of data streams before transmission via fast serial bus.

Data Flow Processing Tools

LocalLink Sequencer is a component for sorting frames from several input interfaces into a single data flow according to the frame sequence numbers. The component is similar to the LocalLink Binder with an extra feature that sorts the frames to their original order.

LocalLink Switch forwards incoming frames to the particular output interfaces according to an information in the frame header. It can be used for switching and easy data replication.

LocalLink Transformer component is used to transform data width of LocalLink packet stream. The supported data bus widths are 8, 16, 32, 64 and 128 bits. The component supports independent write and read clock domains.



Data Storage Components

LocalLink FIFO is an ordinary FIFO with receive and transmit interfaces. It supports the LocalLink optional interface signals SRC_DSC_N and DST_DSC_N (source and destination discontinue), so the FIFO is able to discard the actually receiving or transmitting frame on demand. The type of used memory (BlockRAM or Distributed RAM), data width (8, 16, 32, 64 or 128) and size (number of FIFO items) are fully configurable.

Debug & Simulation Components

LocalLink Watch is a passive probe with an arbitrary number of interfaces. It counts number of passed frames and optionally checks the data flow for violations of protocol specification. Captured data are gathered by a software application.

LocalLink TX and RX buffer are intended for hardware debugging. The TX buffer performs generation of LocalLink flow. A software application prepares the testing data and controls their transmission. The RX buffer performs LocalLink flow capture. Data are gathered by a software application.

LocalLink Simulation Component is intended for simulation purposes. It performs the LocalLink flow generation and capture according to a configuration file.

Other LocalLink Tools

LocalLink Marker is a generic component which is designed for inserting marks into LocalLink frames. The mark can be inserted into an arbitrary position of the frame. For example, the Marker can be used for marking frames with the input interface number, time-stamp or sequence number.

LocalLink Cutter performs inverse functionality to the LocalLink Marker. It removes an arbitrary number of bytes from an arbitrary position in the LocalLink frame.

LocalLink Trimmer is dedicated for removing undesirable part(s) of LocalLink frames (e.g. header, footer or both).

Supported Protocol

The LocalLink tools are fully compatible with the LocalLink required interface specification. For the optional LocalLink interface, the SOP_N, EOP_N and REM signals are supported.

Deliverables

- Fully synthesizable VHDL RTL source code or netlist
- SW applications for debugging components support
- Complete documentation
- Synthesis scripts
- Expert technical support

Recommended Design Experience

HDL coding experience is required to instantiate the cores in a design and familiarity with Xilinx tool flow to successfully place and route the design.

Ordering Information

The LocalLink tools are provided under terms of the SignOnce IP license. Please contact INVEA-TECH for pricing and additional information about this product.

This product is based on the technology transfer from CESNET z.s.p.o.