

Product Brief

Introduction

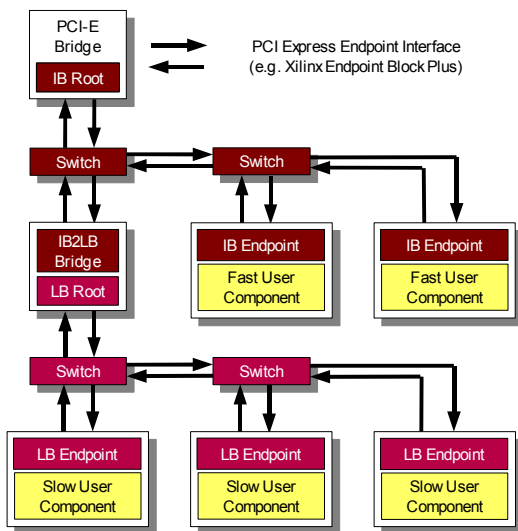
The On-chip interconnection system is a flexible bus architecture which provides complete host bus interface solution. It performs effective data transfers between components within FPGA and host PC memory and also between FPGA components internally. The supported host bus interfaces are PCI, PCI-X and PCI Express x1, x4 and x8.

With time-consuming performance, functional, and timing pattern issues resolved, designers can focus on product differentiation – dramatically reducing costs and time-to-market.

System Architecture

Elements of the On-chip interconnection system include a host bus interface bridge, an Internal bus, a Local bus and DMA controllers. The host bus bridge performs the connection between Internal bus and third-party PCI endpoint blocks. It allows easy interconnection with the Xilinx Endpoint Block Plus for PCI Express or other vendors host bus endpoints.

The Internal and Local bus supports both data transfers between FPGA components and the host RAM, and data transfers between FPGA components internally. High-performance components connect to the high-bandwidth Internal bus. Components that don't require high throughput to the software layer connect to the resource-saving Local bus. Both buses are based on the tree topology and are formed by a root component (serving also as a bridge), switches and endpoints. The system architecture is shown in the following figure.



On-Chip Interconnection System Architecture

Features

- Complete host bus interface solution
- PCI, PCI-X, PCI Express x1, x4, x8 support
- Easy integration with Xilinx Endpoint Block Plus for PCI Express or other vendors host bus endpoints
- Flexible bus architecture
 - High-performance Internal Bus
 - Resource-saving Local bus
- DMA controllers
- No limitation for number of connected components
- Split transactions
- Packet communication
- FPGA suitable tree architecture
 - No on-chip tri-states required
 - Distance non-sensitive
 - Pipelining
- Master/slave option for each endpoint
- Simple and fast simulation models

Performance Features			
Bus type	Local Bus	Internal Bus	Internal Bus
Bus width	16-Bit	64-Bit	128-Bit
Max frequency	125MHz	125MHz	125MHz
Max bandwidth	2Gb/s	8Gb/s	16Gb/s

Target Applications

The On-chip interconnection system is a complete host bus interface solution suitable for all high-performance I/O applications that transfer large amounts of data from adapter into the host RAM and vice versa. Examples of target application areas:

- networking
- telecommunication
- VoIP applications
- cryptography and security
- image and video processing
- bioinformatics

Host Bus Interface Bridge

The Host bus interface bridge represents the root component of the Internal bus tree architecture. It performs the connection between Internal bus and third-party PCI endpoint blocks (Xilinx PCI Express Endpoint Block Plus or others). For example, the PCI-E bridge performs transformation between PCI Express Transaction Layer Packets (TLP) and Internal bus packets.

Internal Bus

The Internal Bus (IB) is a high throughput bus dedicated for transferring of data internally between FPGA components as well as between FPGA components and the PCI interface. The communication protocol is packet based and covers read, write and completion transactions. The Internal bus operates at 125 MHz and the link is either 64 or 128 bits wide and full duplex. These features allows an easy connection to the PCI Express host interface. The tree topology enables the endpoints to communicate with each other in separate branches without wasting the bandwidth of the Internal bus. The IB endpoints can operate in master or slave mode. In the master mode, the bus master operations are supported.

Local Bus

The Local bus (LB) is a resource-saving bus for half-duplex communication with slower components. It is suitable for configuration data transfers or state and debug information reading. It is 16 bits wide operating at 125 MHz clock frequency. The Local bus root is connected with the Internal bus via an IB2LB bridge. Similarly to IB endpoints, LB endpoints can operate in master or slave mode.

DMA Transfers

Both, the Internal and the Local bus master endpoints include DMA controllers. These controllers perform bus master transfers between FPGA components and host RAM as well as between FPGA components internally. The customer can also take advantage of a DMA controller integrated in the host bus interface bridge.

Simulation Models

There are two simulation models available – LB endpoint model and IB transaction model. The LB endpoint model is suited for debugging of local bus connected components. This model implements a set of functions for LB transactions generation. The IBSIM is the second model performing simulation of the Internal bus transactions. It allows to simulate the whole design without time-consuming simulation of PCI endpoint block.

Deliverables

- Fully synthesizable VHDL RTL source code or netlist
- Complete documentation
- Expert technical support

Ordering Information

The On-chip interconnection system is provided under terms of the SignOnce IP license. Please contact INVEA-TECH for pricing and additional information about this product.

This product is based on the technology transfer from CESNET z.s.p.o.